CLAIMS

What is claimed is:

Sub A1

1. A system comprising:

a component;

a detector to detect a power management event; and

a controller to transition, in response to the power management event, a first setting of the component from a first performance mode to a second performance mode,

the controller to transition the component to a reduced activity state, and to change a second setting of the component from a first performance mode to a second performance mode.

2. The system of claim 1, wherein the component is the processor.

3. The system of claim 1, wherein changing the first setting of the component includes changing the core processor supply voltage level from a first voltage level to a second, higher voltage level.

4. The system of claim 1, wherein the reduced activity state includes the sleep state.

5. The system of claim 1, wherein changing the second setting of the component includes changing the core processor clock frequency from a first frequency level to a second, higher frequency level.

6. The system of claim 1, wherein the core processor clock remains active during the sleep state.

7. The system of claim 1, wherein a system clock input to the processor remains active during the sleep state.

8. The system of claim 1, wherein the power management event includes a change of the system power source from an internal power source to an external power source.

Sub A1

9. The system of claim 1, wherein changing the first setting of the component can requires 500 microseconds.

10. The system of claim 1, wherein changing the second setting of the component requires less than 5 microseconds.

11. A system comprising:

a component;

a detector to detect a power management event;

a controller to transition the component, in response to the power management event, to a reduced activity state,

the controller to change a first setting of the component from a first performance mode to a second performance mode,

the controller to transition the component out of the reduced activity state, and to transition a second setting of the component from a first performance mode to a second performance mode.

12. The system of claim 11, wherein the component is the processor.

13. The system of claim 11, wherein the reduced activity state includes the sleep state.

Sub A1

14. The system of claim 11, wherein changing the first setting of the component includes changing the core processor clock frequency from a first frequency to a second, lower frequency.

15. The system of claim 11, wherein changing the second setting of the component includes changing the core processor supply voltage level from a first voltage level to a second, lower voltage level.

16. The system of claims 11, wherein a system clock input to the processor remains active during the sleep state.

17. The system of claims 11, wherein the core processor clock remains active during the sleep state.

18. The system of claim 11, wherein the power management event includes a change of the system power source from an external power source to an internal power source.

19. The system of claim 12, wherein changing the first setting of the component requires less than 5 microseconds.

20. The system of claim 11, wherein changing the second setting of the component can requires 500 microseconds.

21. A computer-readable medium having stored thereon a set of instructions to translate instructions, the set of instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event;

transitioning a first setting of a component from a first performance mode to a second performance mode in response to the power management event,

Sub A1

transitioning the component to a reduced activity state, and to change a second setting of the component from a first performance mode to a second performance mode,

if the power management event includes the system power source switching from an internal power source to an external power source; and

transitioning the controller to a reduced activity state in response to the power management event,

changing the second setting of the component from the second performance mode to the first performance mode,

transitioning the component out of the reduced activity state, and transitioning the second setting of the component from the second performance mode to the first performance mode,

if the power management event includes the system power source switching from an external power source to an internal power source.

22. The computer-readable medium of claim 21, wherein the first setting of the component includes the core processor supply voltage level.

23. The-computer readable medium of claim 21, wherein the component is the processor.

24. The computer-readable medium of claim 22, wherein the second performance mode includes a higher voltage level than the first performance mode.

Sub A1

25. The computer-readable medium of claim 21, wherein the reduced activity state includes the sleep state.

26. The computer-readable medium of claim 21, wherein the core processor clock remains active during the sleep state.

27. The computer-readable medium of claim 21, wherein the second setting of the component includes the core processor clock speed.

28. The computer-readable medium of claim 27, wherein the second performance mode includes a higher frequency level than the first performance mode.

29. The computer-readable medium of claim 21, wherein a system clock input to the processor remains active during the sleep state.

30. The computer-readable medium of claim 21, wherein changing the second setting of the component requires 500 microseconds.

31. An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller to transition, in response to the indication, transition a power supply voltage level of a component from a first level to a second, higher level,

the controller to transition the component to a low activity state, and to change a core component clock frequency from a first level to a second, higher level, while the component is in the low activity state.

32. The apparatus of claim 31, wherein core component clock and a system clock input to the component remain active during the low activity state.

33. The apparatus of claim 31, wherein the indication is generated in response to a change in a power source in the system from an internal power source to an external power source.

34. An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller to transition the component to a low activity state in response to the indication,

the controller to change the component core clock frequency from a first level to a second, lower level, while the component is in the low activity state,

the controller to transition the component out of the reduced activity state, and to transition a power supply voltage level of the component from a first level to a second, lower level.

35. The apparatus of claim 34, wherein the core component clock and a system clock input to the component remain active during the low activity state.

36. The apparatus of claim 34, wherein the indication is generated in response to a change in a power source in the system from an external power source to an internal power source.